Fully Flexible Solution-Deposited ZnO Thin-Film Transistors

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Electronic systems on flexible substrates posses the advantage of mechanical flexibility in actual use, but also provide more rugged rollable devices and may therefore result in lower manufacturing costs associated with continuous roll-to-roll fabrication. To realize these advantages of flexible electronics, low-temperature solution processing is strongly desirable. In this regard, organic semiconductor materials have been extensively researched.[1] Organic semiconductor polymers are soluble in a variety of solvents, and small molecules can be derivatized to soluble precursors. Organic transistors can also be fabricated by solution processing near room temperature,[2] compatible with temperature-sensitive plastic substrates.[3–5] Despite successful demonstrations of flexible organic electronics, however, they are generally sensitive to operating conditions and are unstable during long-term operation.[6]

Recently, the materials science community has paid considerable attention to new solution-processable inorganic semiconductors to realize high-performance devices. Grüner and co-workers investigated carbon nanotube-based thin film transistor (NTTFT) devices on a plastic surface. These devices were composed of sprayed nanotube networks at appropriate densities, and their performances did not degrade significantly by bending or mechanical deformation.[7] Other inorganic materials including chalcogenide compounds have been applied to transistor fabrication using solution-deposition, but they were made on rigid substrates.[8] On the other hand, the dry transfer process provides an efficient approach for the relocation of high-quality inorganic semiconductors from inorganic substrates to plastic substrates using polymeric stamps.[9,10] However, this technique is complicated, requiring a multi-step integration, and may suffer from inferior contact with the electrode during semiconductor transfer to the device substrate.

Flexible transistors with Zn-based oxide materials as an active layer have been recently investigated.[11,12] The high mobilities of electrons in disordered amorphous Zn-based oxide materials arise from the overlap of the non-directional *n*s orbitals of transition metal cations, thereby creating a conduction band regardless of the angle between nearest neighbors (here, *n* is the principal quantum number).[11a,13] This confers attractive properties on amorphous oxide semiconductors, such as low-temperature processability and compatibility with mechanically flexible substrates. Carcia et al. reported the first demonstration of zinc oxide (ZnO) flexible transistors deposited by RF magnetron sputtering near room temperature.[14] However, detailed bending tests simulating practical and realistic uses have yet to be performed. We previously demonstrated the feasibility of solution-processed high-performance flexible ZnO-TFTs.[15] Direct dissolution of zinc hydroxide in aqueous ammonia allowed for rapid metal-ammine dissociation and simple dehydration/condensation reactions yielding nanocrystalline ZnO at 140 °C. Here, we focused on the influences of the various bending tests, to determine if the solution-processed ZnO-TFTs are bendable, rollable, wearable, and foldable. This proof-of-concept study is a step toward "flexible applications".

We fabricated ZnO-TFTs in bottom-gate and top-contact configurations using 50-μm-thick polyimide (PI) substrates (for more details, see Experimental section). Indium tin oxide (ITO, Sn 5%), which served as a common gate electrode, was deposited on PI by a sputter. A 270-nm-thick SiO_2 gate insulator was deposited by plasma enhanced chemical vapor deposition (PECVD) at 200 °C. The ZnO layers were then obtained by spin-coating the Zn aqueous solution, followed by annealing in a convection oven at 200 °C for 2 h. Aluminum (Al) source and drain electrodes were thermally evaporated onto the ZnO film using a shadow mask (**Figure 1a**). Figure 1b shows the electrical characteristics of solution processed ZnO-TFTs having a channel width of 1500 μm and a length of 120 μm. The transfer characteristics of ZnO-TFTs on flexible substrates show a lower off-current on the order of $<10^{-12}$ A and an on-off current ratio of ~10^6. The estimated saturation mobility was 0.35 $cm^2\ V^{-1}\ s^{-1}$, and the threshold gate voltage was positive (V_T ~ +6.7 V), suggesting that our flexible ZnO-TFT operates in the enhancement mode.

Figure 1c shows typical output characteristic of the solution-processed flexible ZnO-TFT. The drain current (I_{DS}) abruptly increases as the drain voltage (V_{DS}) increases at a positive gate bias (V_{GS}), indicating that electron carriers are mainly generated. Furthermore, the output characteristic exhibits a clear pinch-off and drain current saturation, and the output characteristic shows good contact performance at low drain voltages, indicating that the electron carriers injected from the electrode can easily overcome the energy barriers (ϕ_{Be}) at the electrode-semiconductor interface.[16] Figure 1d shows the flexible TFT array rounded at a 7 mm radius, containing 48 TFTs in an area of 7 cm × 7 cm. Survival yield reaches ~96%. Among the

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DOI: 10.1002/adma.201002163

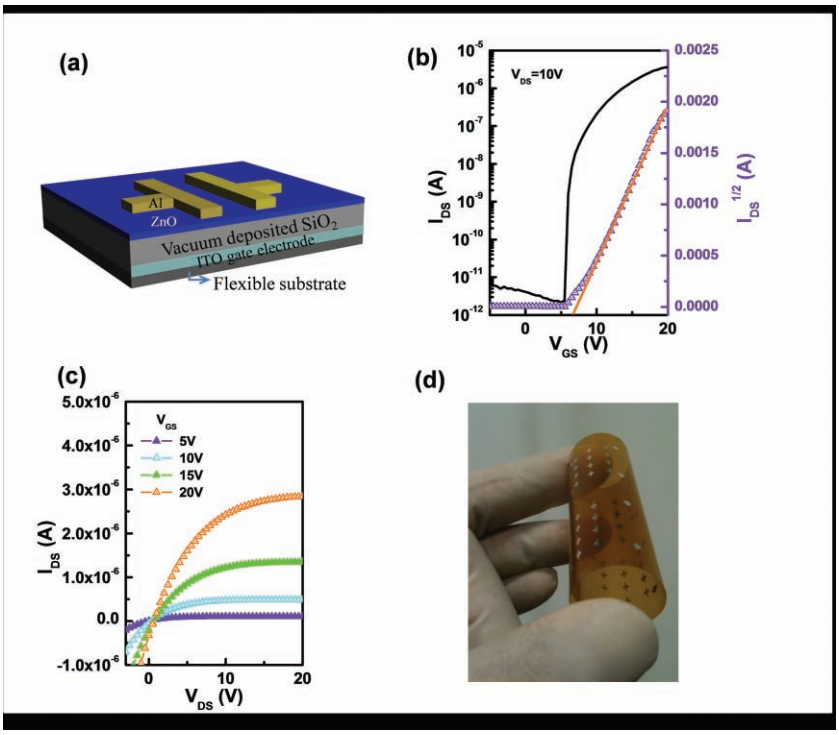

Figure 1. Low-temperature solution-processed ZnO thin film transistors (TFTs) on flexible substrates and their electrical characteristics. (a) Bottom-gated top-contact flexible device configuration. (b) Electrical transfer characteristics of solution-assisted flexible TFTs with a channel width of 1500 μm and a length of 120 μm (at V_{DS} = 10 V), and (c) the corresponding output characteristics from 5 to 20 V of V_{GS} in steps of 5 V. (d) Optical image of 48 solution-processed TFT arrays being rounded into a 7 mm radius.

48 TFTs, only two TFTs failed due to electrical shortages between the gate and the source electrodes. The mobilities and the threshold voltages for the 48 TFTs are shown in the Supporting Information (Figure S1). The average field effect mobility and threshold voltage were 0.27 ± 0.03 cm^2 V^{-1} s^{-1} and 3.3 ± 1.1 V, respectively. Lower mobility and larger variation in threshold voltage are attributed to the oxide-quality of low-temperature deposited SiO_x dielectrics. In general, the silicon oxide gate dielectric is deposited at the temperature above 300 °C by plasma enhanced chemical vapor deposition (PECVD). The reduction in the temperature leads to a change in the deposition mechanism and incorporates a variety of undesirable Si-OH and Si-H bonds, which are responsible for lower film density and higher defect concentrations.[17] Furthermore, low-temperature PECVD SiO_x suffers from thickness variation. These would induce the variations in the TFT electrical parameters. We analyzed the transistors fabricated on thermally grown SiO_2 dielectric that is more dense and less defective. The average field effect mobility and threshold voltage were 0.39 ± 0.03 cm^2 V^{-1} s^{-1} and 5.4 ± 0.4 V, respectively. The average mobility is higher and narrow variations in the electrical parameters are observed. This indicates that low temperature grown SiO_x leads to broad variations and degraded electrical parameters.

The cross-sectional HRTEM images of **Figure 2** reveal that the solution-processed ZnO-TFTs on flexible substrates maintain coherent interfaces without interlayer defects and/or delamination. The thickness of the ZnO active layer was 8 nm (Figure 2b). The ZnO layer annealed at 200 °C in a convection oven was quasi-amorphous, as confirmed by its fast Fourier transformation (FFT) pattern (Figure 2b inset), in contrast to ZnO processed via microwave-assisted annealing at similar conditions.[15] To further confirm the crystalline phase, high resolution X-ray diffraction (XRD) was performed for the single-coated ZnO layer. The resulting diffraction profile indicated that the ZnO film annealed at 200 °C was mostly amorphous, with a weak wurzite ZnO crystalline peak, as shown in Figure 2c, which is in good agreement with the HRTEM results.

For practical applications, flexible devices should be bendable, rollable, wearable, and foldable without sacrificing their electrical performance. However, there are only a few reports on the flexible characteristic of nanotube- or organic transistor-based TFTs, and these only show simple results before and after bending at different radii of curvature.[18,19] To prove the

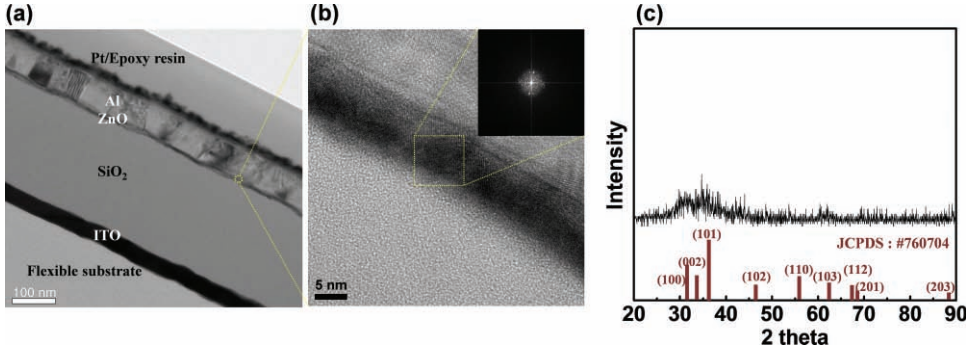

Figure 2. Structural analysis of solution-deposited flexible ZnO TFTs. (a) High resolution transmission electron microscopy (HRTEM) image showing the cross section of the flexible TFTs. (b) Magnified HRTEM image shows a quasi-amorphous phase of the ZnO semiconductor annealed at 200 °C in a convection oven. The inset is the fast Fourier transform (FFT) patterns obtained from the marked image. (c) An XRD profile of the single-coated ZnO layer. The dark red lines represent the hexagonal ZnO structure (JCPDS no. 760704).

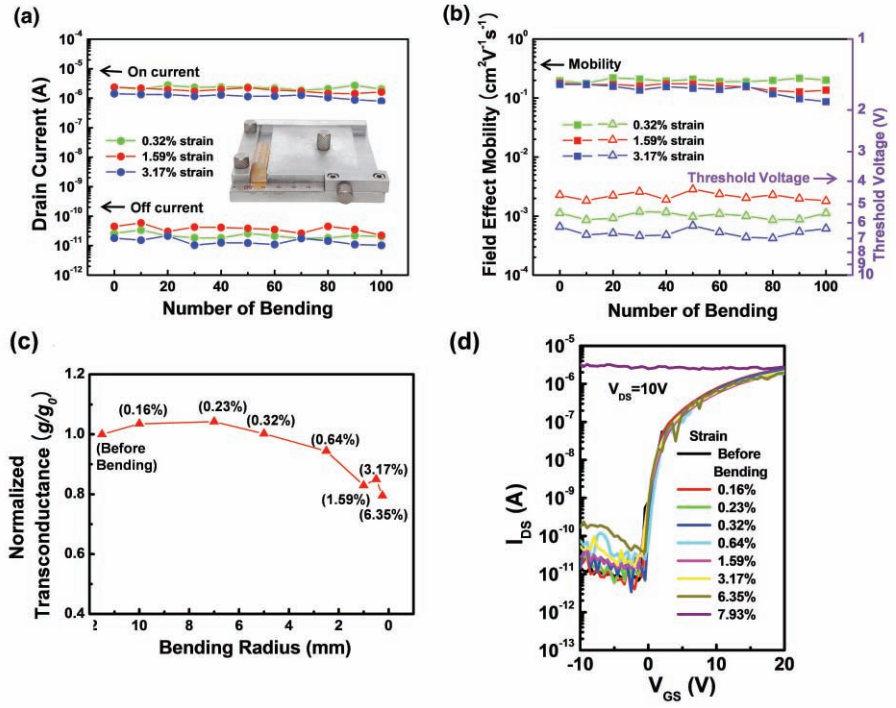

Figure 3. Electrical analysis of the flexible devices under various strain conditions. The variations in the electrical parameters, (a) on and off current, (b) field effect mobility and threshold voltage, shown during the repeated bending cycles under different strains (0.32%, 1.59%, and 3.17%). (c) The change in the normalized transconductance (g/g_o) of a ZnO flexible transistor as a function of bending radius. Estimated strain is represented in parentheses. (d) Transfer characteristics of the ZnO TFT as a function of the strain value. All measurements were instantaneously performed after a bending duration of approximately 1 h, as the strains were varied (the measured bending radii were changed from 10 mm to 0.2 mm).

concept of fully flexible TFTs, we examined the variations in electrical parameters for solution-processed ZnO TFTs that are bent between two parallel plates (see **Figure 3a** inset).[20] Upon bending, the outer surface of the sample was loaded with regard to tension and the inner surface with regard to compression. The electrical parameters are monitored as a function of the radii of curvature as the flexible TFTs are subjected to multiple bending cycles. Bias stress instability may result in unreliable electrical parameters upon repeated bending cyclic tests if the flexible device is electrically unrecovered. Therefore, before the flexible tests, we evaluated the effects of multiple sweep measurements and threshold shifts as a function of relaxation time, after applying a constant gate bias stress (see Figure S2 in Supporting Information). Every ten repeated bendings were therefore performed at an interval of 60 min for better determination of bending influences on the flexible device.

Figure 3a and b show the changes in the electrical parameters such as on–off current, field effect mobility, and threshold voltage during repeated bending cycles at different radii of curvature (i.e., with the solution-processed transistors on the 50-μm-thick substrate, bent with radius R varying from 5 to 0.5 mm, which correspond to tensile strains from 0.32% to 3.17%; for strain calculation, see the Experimental section). Compared to the initial state, the electrical parameters remained nearly unchanged during repeated bending, up to a tensile strain of 1.59%, whereas slight decreases in both the drain current (I_{DS}) and the field effect mobility were observed at a tensile strain of 3.17% after 80 repeated bending cycles. This degradation might be caused by induced interfacial strain near the dielectric after acute bending.[18] Figure 3c shows the normalized transconductance (g/g_o) of soluble ZnO TFT as a function of bending radius. The substrates were held in "bent" positions for approximately 1 h at each measured radius. Although the transconductance of our TFT was decreased by approximately 20% at a radius of 0.25 mm (the tensile strain corresponding to 6.35%), it was possible to operate the device successfully. as shown in Figure 3d. Decrease in the drain current may be attributed to enhanced electron scattering from strain-induced defects formed in the semiconductor.[21] It should be noted that no other flexible transistors including organic semiconductors can survive at a tensile strain of 6.35%. The critical fracture strains for other materials used for flexible TFTs are 1.4% for μs-Si, 1.2% for GaAs,[22] 1–2% for polysilicon,[23] 1.4% for pentacene,[24] 1.18% for single crystalline rubrene,[18] and 3.5% for carbon nanotubes (Please note these values are for the transistor devices, not for materials themselves).[9a,25] The exceptional mechanical properties of our semiconductor may come from its ultrathin thickness (~8 nm) and/or its amorphous-like characteristics.[18,25a] However, when the strain reaches 7.93%, the device fails irreversibly due to the occurrance of large currents between the source/drain and the gate (see Supporting Information, Figure S3). The abrupt increase in the gate current likely results from strain-induced physical damage or fracture of gate insulator.

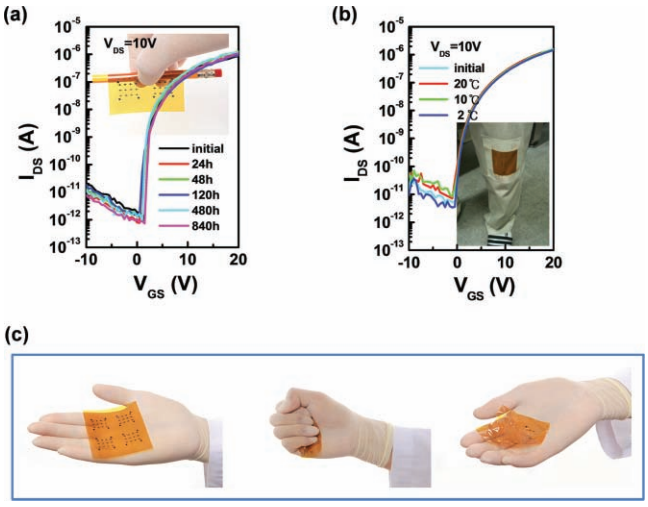

Figure 4. Electrical characteristics and "real-life flexibility tests" of the ZnO-TFTs without passivation, subjected to various bending conditions. (a) Variations in the transfer charateristics over a long bending period (while wrapped around a pencil). Even though the flexible device was mechanically stressed for approximately a month, no electrical parameters changed. (b) One array of 48 TFTs on a flexible large-area substrate was virtually characterized for "wearable applications" under different temperatures and humidities. The survival yield is 72%. We observed that electrical parameters of almost TFTs are not nearly degradable and are very stable. (c) Demonstration of the foldable test. Flexible arrays were repeatedly crumpled in the palm of the hand.

Figure 4a shows the long term performance stability if the device is wrapped around a pencil (diameter of 10 mm) at room temperature in air. There was no noticeable degradation over a month. We also investigated the performance of an array of flexible TFTs on a large-area substrate under simulated wearable conditions. As shown in the Figure 4b inset, the sample was attached to the knee joint, the most active part of the body. The person wearing the device walked for 4 h on days with different ambient temperatures of 2 °C, 10 °C, and 20 °C. Our devices without passivation were surprisingly stable, although the off current slightly varied compared to its initial value. We performed a folding test as shown in Figure 4c. To observe the foldable behavior of flexible FETs, we fabricated a flexible array containing 48 TFTs with patterned gate electrodes in an area of 7×7 cm^2 (see Supporting Information, Figure S4). This flexible array was repeatedly crumpled within the palm of the hand. Even during this severe mechanical stress, the half of the devices operated well, although some failed due to cracking in either the electrode or the gate insulator.

In conclusion, we report on fully flexible solution-processed ZnO thin-film transistors (TFTs) that were subjected to a variety of virtual experiences of flexible applications. Our flexible devices are exceptionally stable against various bending stresses and are bendable, rollable, wearable, and foldable, exhibiting no degradation at tensile strains up to 6.35%. XRD and HRTEM analyses confirmed that the unprecedented flexibility of the solution-deposited ZnO TFTs originates from the formation of an ultrathin, conformable, coherent semiconductor layer with an amorphous-like phase on the plastic substrate. Thus, our solution processable semiconductor devices can be used to realize transparent, flexible solution-processed oxide devices.

Experimental Section

Synthesis of ZnO materials: Sol solutions (0.1 M) for the ZnO layer were prepared by directly dissolving zinc hydroxide ($Zn(OH)_2$, 98%, Junsei, Japan) in an aqueous ammonia solution (NH_4OH, 99.999%, Alfa Aesar), resulting in a solution of pH 13.5. Prior to coating, the formulated solution was rigorously stirred for ~12 h at room temperature and filtered through 0.2 μm membrane filters.

Device fabrication and characterization: To determine the electrical properties of the optimal gate dielectric for low-temperature processing (200 °C), a low-temperature processed dielectric film on heavily-doped n^+-Si was covered with a Au top electrode. Our optimally deposited dielectric film at 200 °C showed good leakage resistance, and the dielectric constant at 1 MHz was also measured as 3.2 (capacitance = 10.5 nF/cm^2). The synthesized ZnO solution was spin-coated at the speed of 2000 rpm for 25 s onto SiO_x (PECVD grown at 200 °C, thickness (t) = 270 nm)/ITO(t = 50 nm)/PI(t = 50 μm) substrate. The coated ZnO layers were annealed at 200 °C for 2 h in a convection oven (BPG-9050A, Neuron Fit Co., Ltd.). To fabricate the transistor with top-contact electrodes, an Al source and drain electrodes of 50 nm in thickness were deposited by thermal evaporation (pressure ~10^{-6} Torr) through a shadow mask. The width of the channel was 1500 μm, and the length of 120 μm was used. The *I–V* characteristics of all transistors were measured in the dark in ambient air using an Agilent 4155C semiconductor parameter analyzer to determine the electrical performances of the transistors. The threshold voltage (V_T) was determined from $(I_{DS})^{1/2}$ vs V_{GS} plots. The saturation mobility (μ_{sat}) was calculated from the following formula:

$$I_{DS} = \left(\frac{\mu_{sat} C_i W}{2L}\right)(V_{GS} - V_T)^2$$

where C_i, W, and L are the capacitance of the gate dielectrics per unit area, the channel width and length, respectively.[16] The microstructure of the ZnO film was investigated using high resolution transmission electron microscopy (HR-TEM, JEM-2100F, JEOL) and by a high resolution X-ray diffraction using Cu K radiation (X PET-PRO MRD, Phillips). All the bias stress measurements were carried out at room temperature, in air and in the dark. Gate bias stress was performed for a predetermined time with the bias stress voltage in the linear regime using a V_{DS} of 1 V instead of in the saturation regime, where the effect of bias stress on the threshold voltage shift is smaller.[26] The transfer characteristics were measured before and after applying the stress, during the gate voltage sweep (from −10 V to 20 V). The bending tests were performed between two parallel plates with radius R varying from 10 to 0.2 mm, corresponding to a tensile strain of 0.16% to 7.93%. We performed the electrical measurement for the transistors located in the center portion between the two plates where was representative of maximal strain in the sample. In addition, the estimated strain value for the film layer placed onto a compliant substrate is given by the following equation: $\varepsilon = [(d_f + d_s)/2R]\ [(1 + 2\eta + \chi\ \eta^2)/\{(1 + \eta)(1 + \chi\ \eta)\}]$, where ε is the strain, R is the bending radius, $\chi = Y_f/Y_s$ (Y_f and Y_s are the Young's moduli of the film layer and the substrate, respectively), and $\eta = d_f/d_s$ (d_f is the thickness of the film layer and d_s is the thickness of the substrate). Here, the thickness of the compliant substrate and the films are 50 μm and ~0.3 μm, respectively, and the Young's modulus term, χ, is ~100.[25] In addition, virtual flexible tests such as multiple bending, rollable, wearable, and foldable tests were performed in ambient conditions (at room temperature in open air without passivation).

Supporting Information

Supporting information is available online from Wiley Online Library or from the author.

Acknowledgements

This work was supported by Mid-career Researcher Program through NRF grant funded by the MEST (Nos. 2009-0086302). It was also partly supported by the Second Stage of the Brain Korea 21 Project.

Received: May 4, 2010
Revised: June 12, 2010
Published online: August 23, 2010

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